

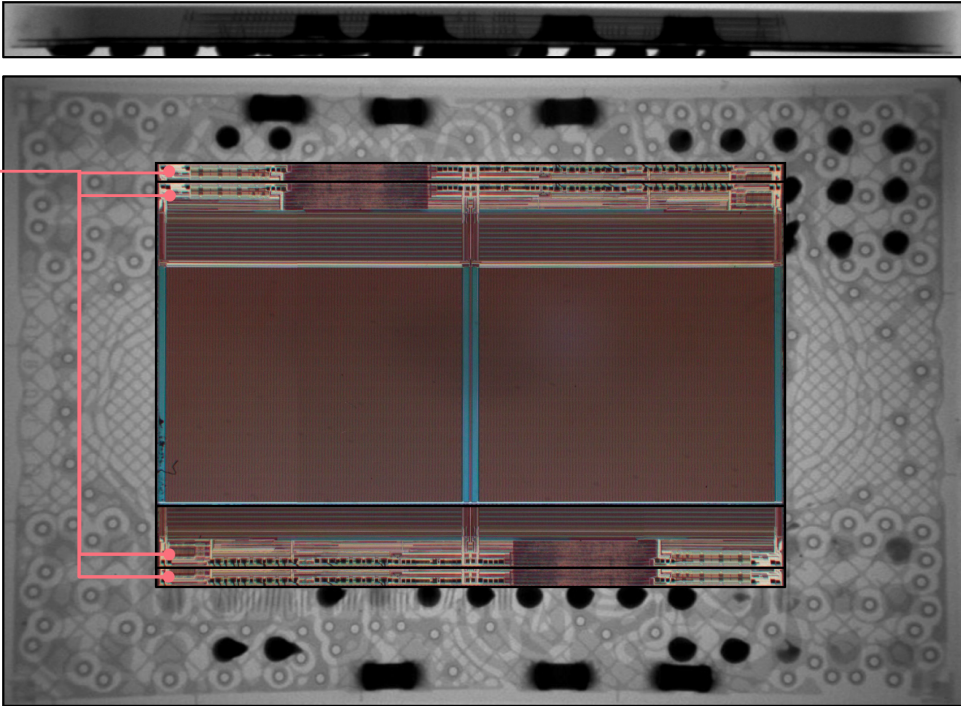
EXHIBIT G

U.S. Patent No. 6,724,241 (“’241 Patent”)

Western Digital products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the WD Ultrastar SN630 WUS3BA196C7P3E3 (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent. While the infringing structure and functionality of the Accused Products is illustrated below using the WD Ultrastar SN630 WUS3BA196C7P3E3 as an example, all Accused Products operate in substantially the same way for purposes of infringement.

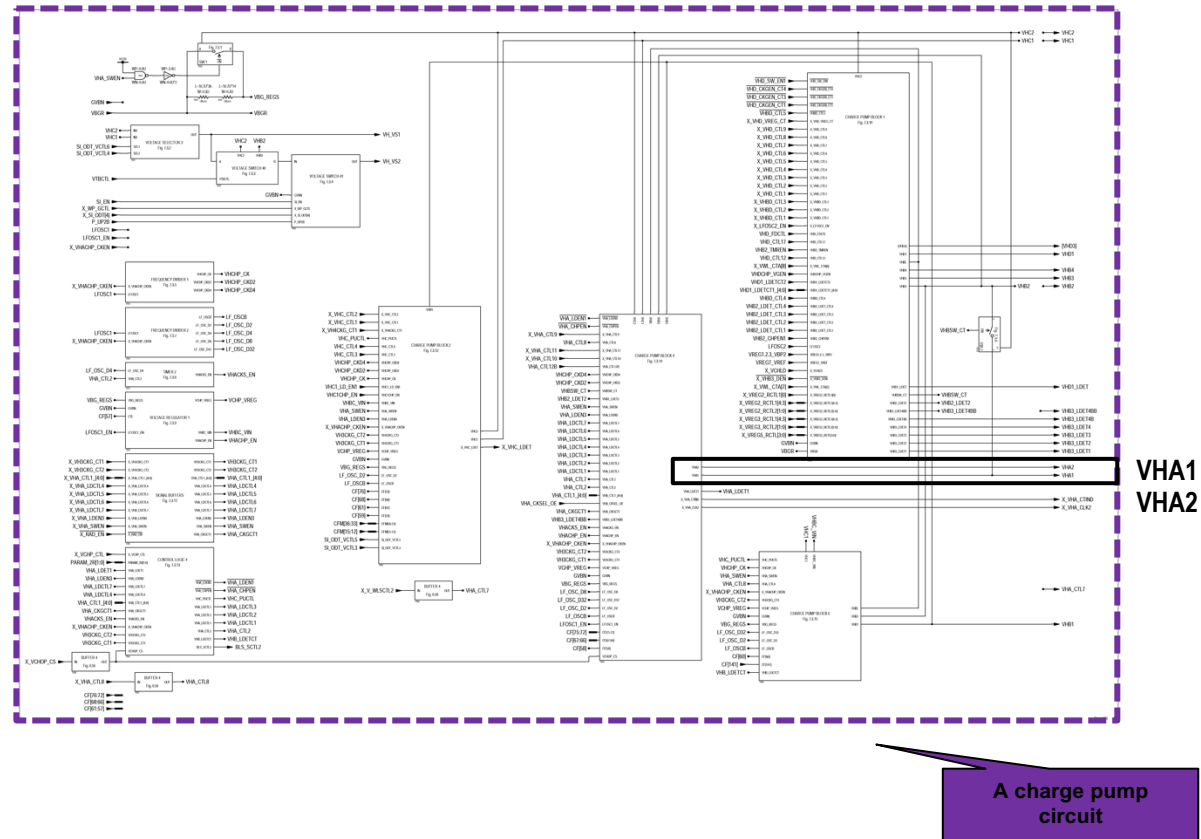
Claim 1

Claim 1	Accused Products
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the WD Ultrastar SN630 WUS3BA196C7P3E3 includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

Claim 1	Accused Products
	<div data-bbox="653 272 888 365"><p>9 - SanDisk #15175-128G ? Multichip Memory - 128 GB 3D TLC NAND Flash (4-Die Pkg.) Pkg Size: 18 x 12 mm</p></div> <div data-bbox="653 418 921 495"><p>9.1 - SanDisk #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.16 x 6.27 mm</p></div> <div data-bbox="667 971 842 1010"><p>Function: Memory: Non-Volatile</p></div> <div data-bbox="926 289 1881 990">A microscopic image of a circuit board, likely a hard drive controller or memory module. A red rectangular box highlights a specific area on the board, which contains several integrated circuits. Two red lines point from the text boxes on the left to the highlighted area. The board itself has a complex pattern of components, including capacitors and other chips.</div> <div data-bbox="636 1027 1764 1062"><p>Source: TechInsights Deep Dive Teardown, WD Ultrastar SN630 WUS3BA196C7P3E3</p></div>

Claim 1

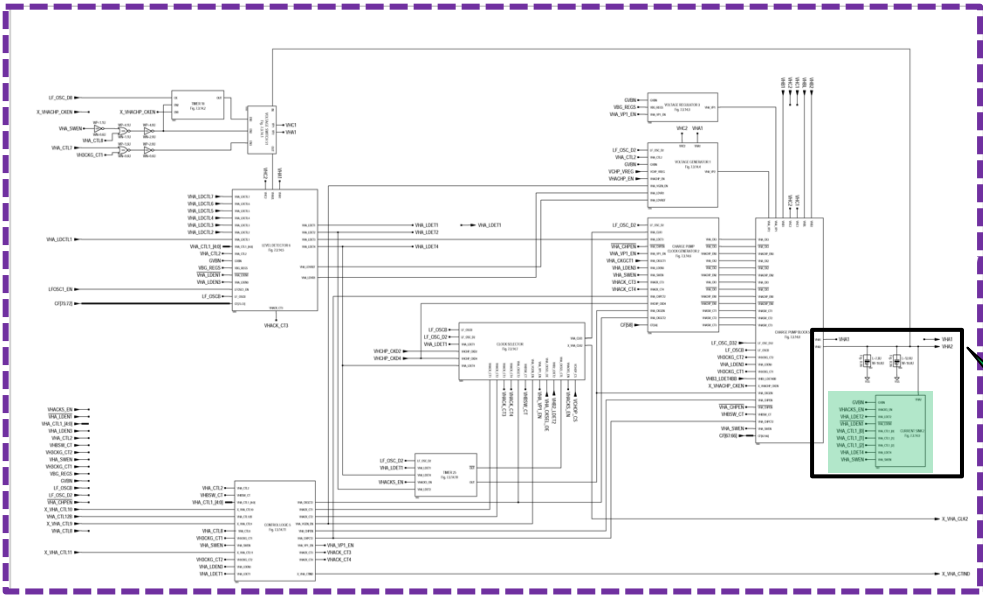
Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System

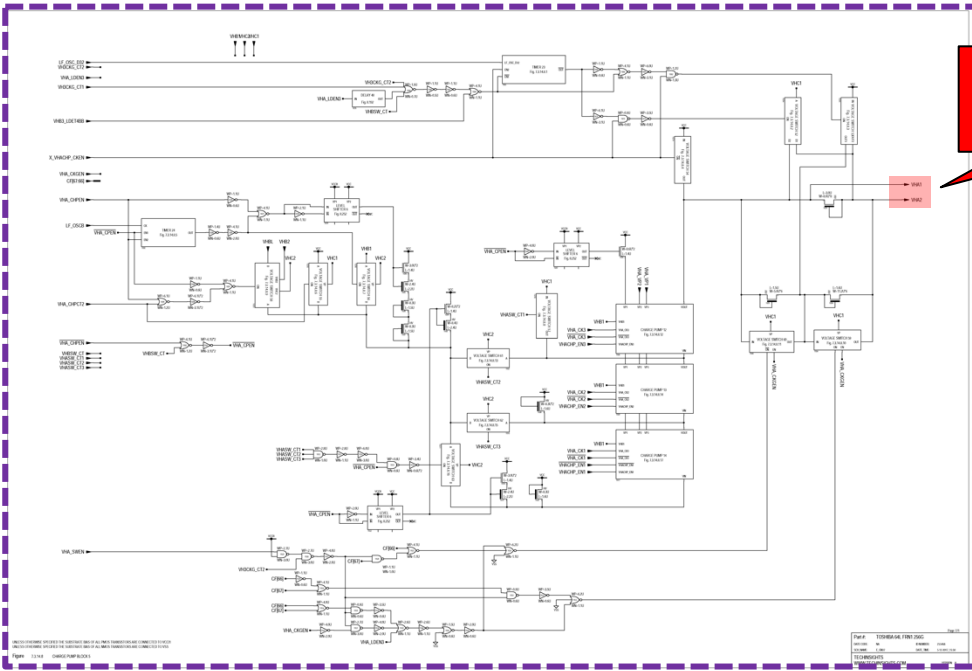
Claim 1

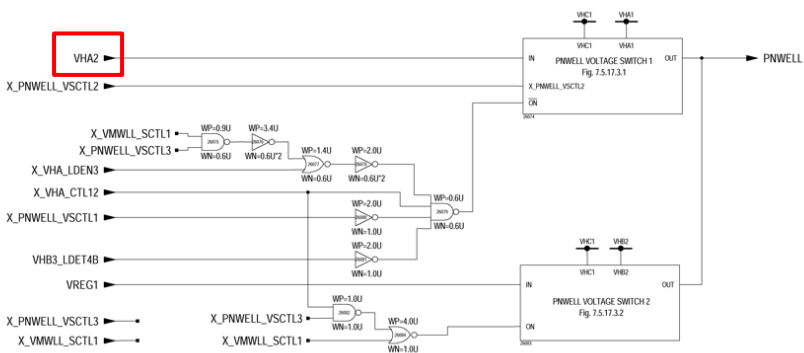
Accused Products

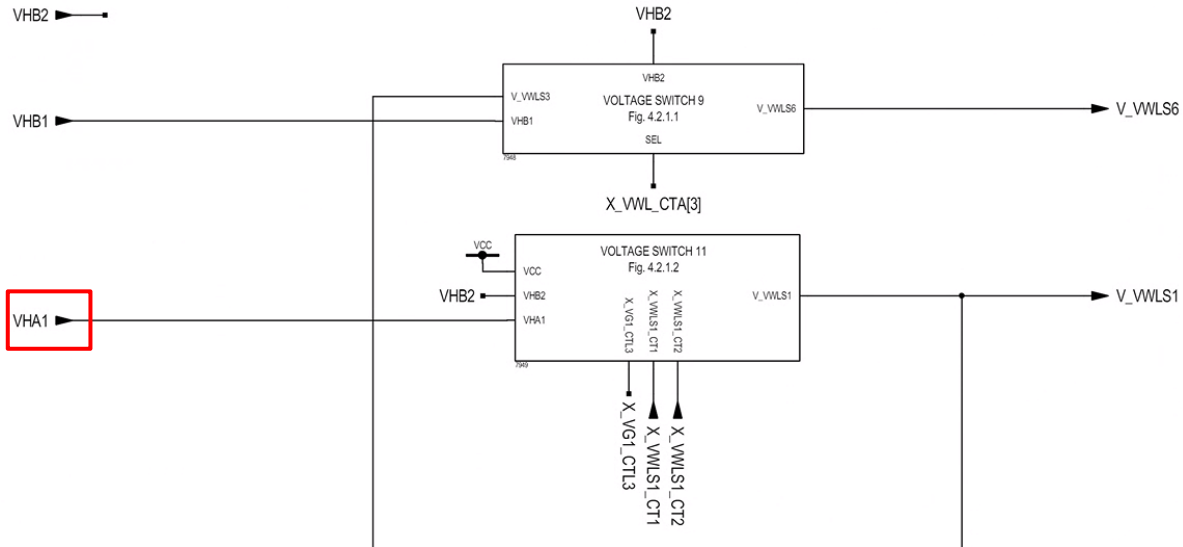


having minimal voltage ripples

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

Claim 1	Accused Products
	<div data-bbox="640 267 1606 933"></div> <div data-bbox="1591 310 1871 418" style="background-color: red; color: black; padding: 5px;"><p>for generating a charge pump voltage (VHA1, VHA2)</p></div> <div data-bbox="1623 483 1843 581" style="background-color: white; border: 1px solid black; padding: 5px;"><p>VHA1 and VHA2 are driven by the same pumping circuit</p></div> <div data-bbox="1627 651 1841 716" style="background-color: purple; color: white; padding: 5px;"><p>A charge pump circuit</p></div>
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5	

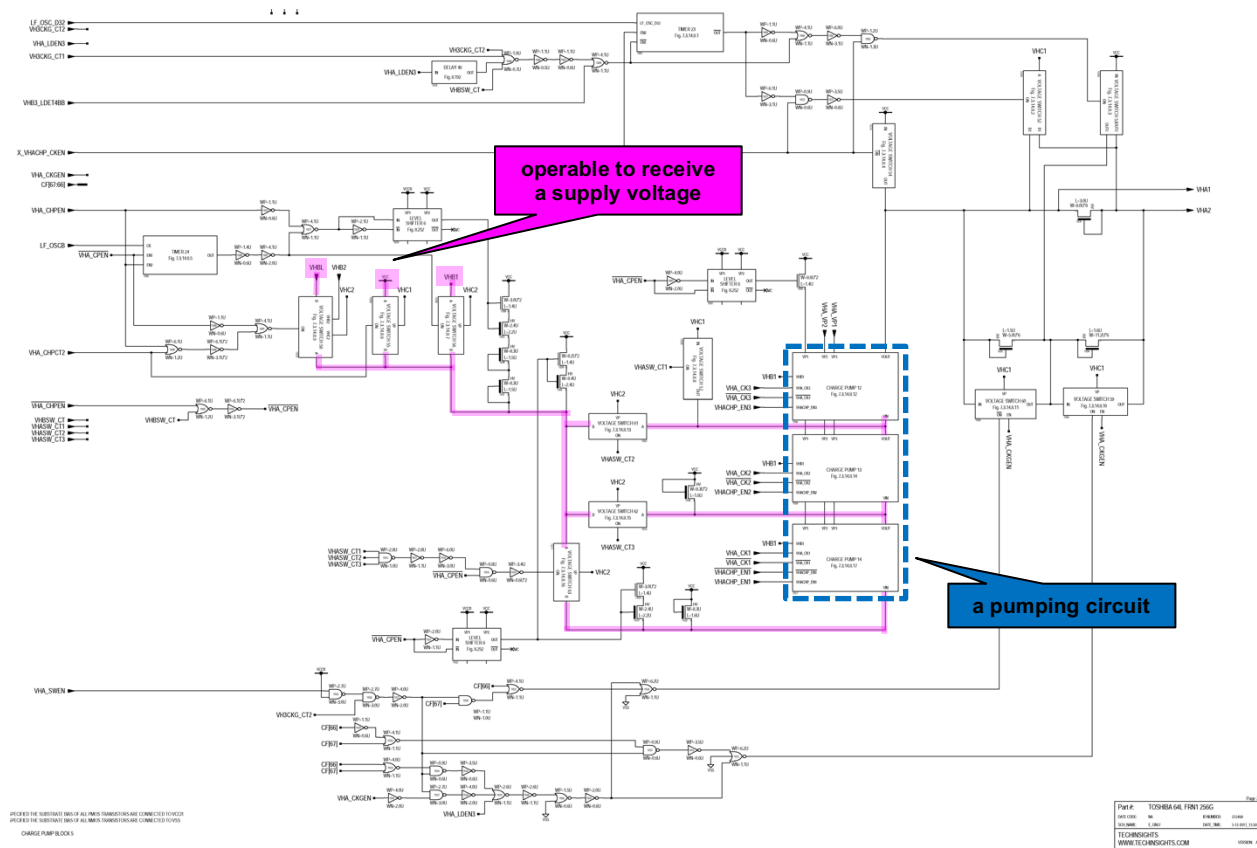
Claim 1	Accused Products
	<p data-bbox="674 300 1241 362">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>  <p data-bbox="632 829 1829 901">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Products
	<p>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>[1a] a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit of the WD Ultrastar SN630 WUS3BA196C7P3E3, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72)</p>

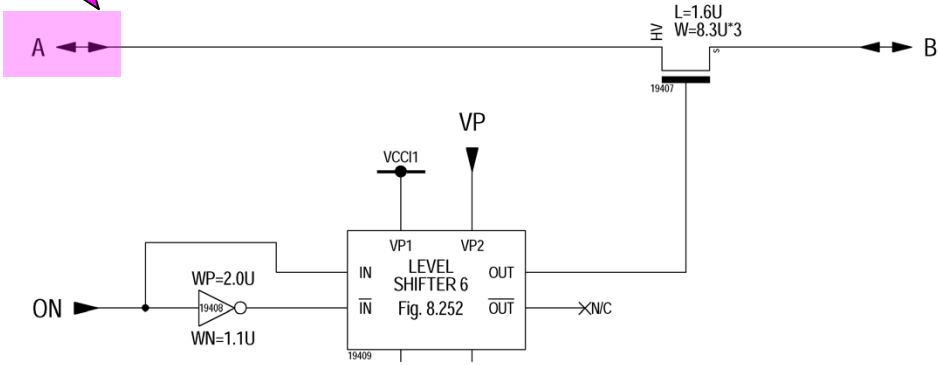
Claim 1	Accused Products
	<p>adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

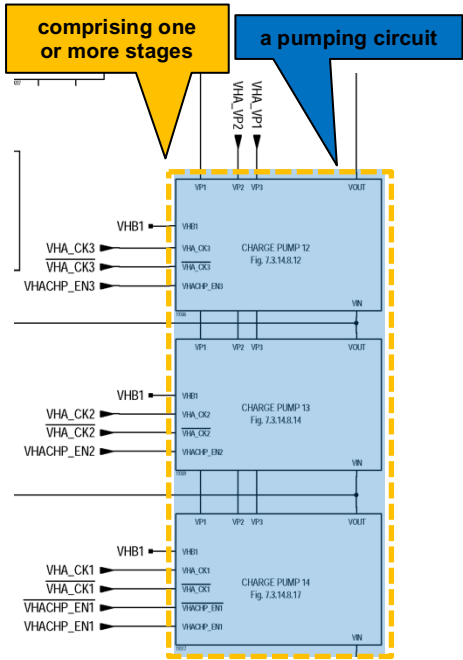
Claim 1

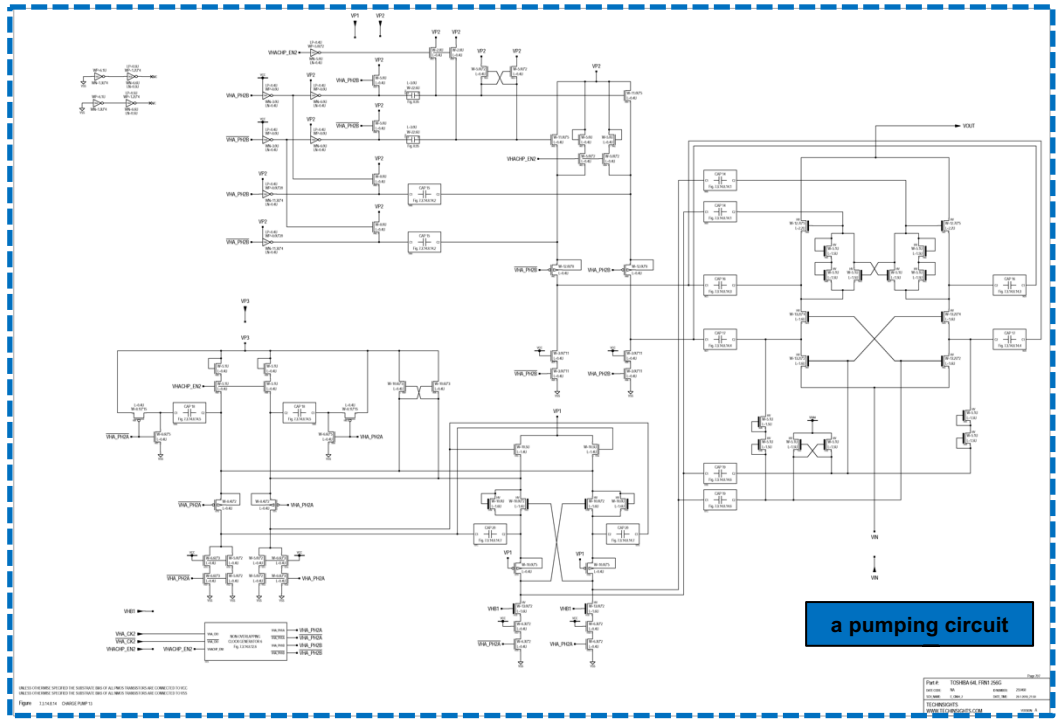
Accused Products

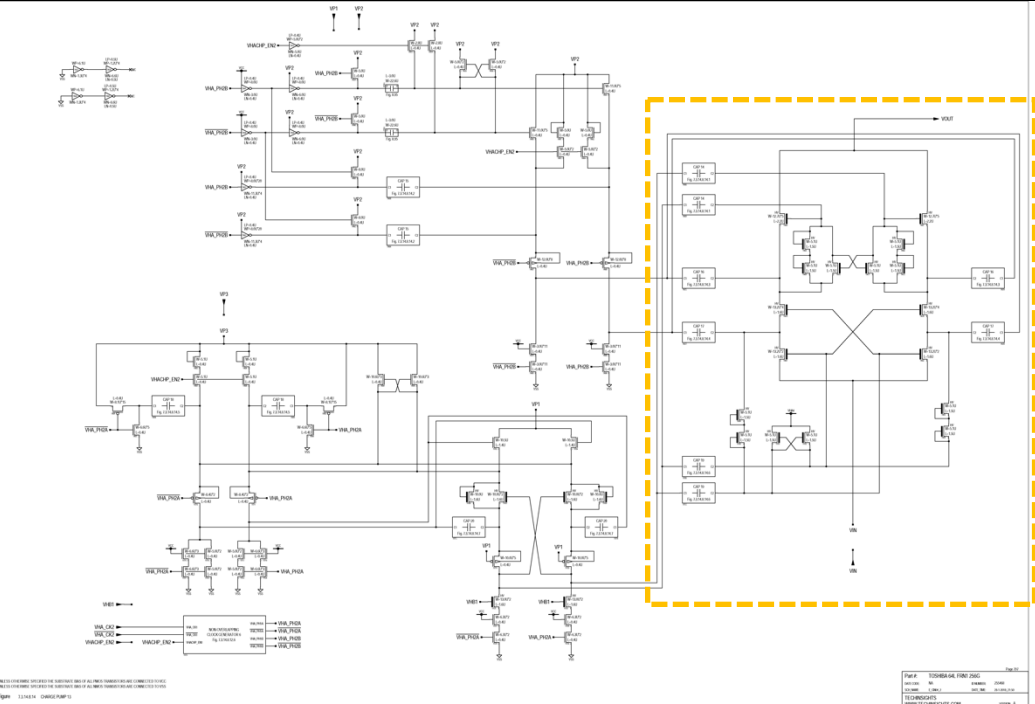


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Products
	<div data-bbox="632 259 963 326" style="background-color: #FF00FF; color: black; padding: 5px; border: 1px solid black;"> operable to receive a supply voltage (VCC) </div> <div data-bbox="697 396 814 462" style="background-color: #FFB6C1; color: black; padding: 5px; border: 1px solid black; display: inline-block;"> A </div>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

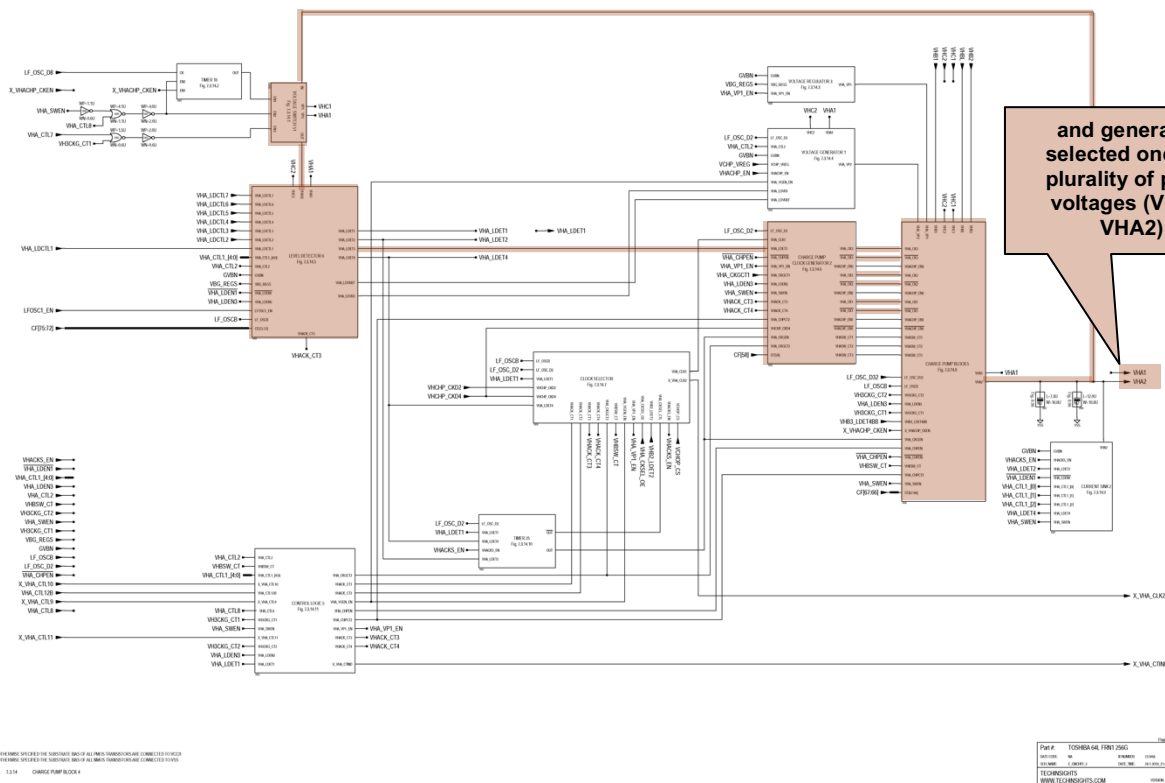
Claim 1	Accused Products
	 <p>The diagram illustrates three stacked charge pumps, labeled CHARGE PUMP 12, CHARGE PUMP 13, and CHARGE PUMP 14. Each pump is represented by a blue rectangular block with internal circuitry. The pumps are connected in series, with the output of one pump serving as the input for the next. The top pump (12) has inputs VP1, VP2, and VP3, and an output VOUT. The middle pump (13) has inputs VP1, VP2, and VP3, and an output VOUT. The bottom pump (14) has inputs VP1, VP2, and VP3, and an output VOUT. The pumps are connected to a common ground (VSS) and a common power supply (VDD). The diagram includes callouts: a yellow callout pointing to the top pump labeled 'comprising one or more stages' and a blue callout pointing to the top pump labeled 'a pumping circuit'. The diagram also shows various control signals: VHB1, VHA_CK3, VHA_CK2, VHA_CK1, VHA_OK3, VHA_OK2, VHA_OK1, VHACP_EN3, VHACP_EN2, VHACP_EN1, and VHACP_EN0. The diagram is identified as Figure 7.3.14.8 Charge Pump Block 5.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

<p>Claim 1</p>	<p>Accused Products</p>										
	 <p data-bbox="1436 862 1659 906">a pumping circuit</p> <table border="1" data-bbox="1551 935 1671 980"> <tr> <td>Part:</td> <td>05138-064G 3D NAND</td> </tr> <tr> <td>Rev:</td> <td>1.0</td> </tr> <tr> <td>Author:</td> <td>TECHINSIGHTS</td> </tr> <tr> <td>Rev:</td> <td>1.0</td> </tr> <tr> <td>File:</td> <td>05138-064G 3D NAND</td> </tr> </table> <p data-bbox="636 943 825 971"> <small> This circuit diagram is provided for information only. It is not intended to be used as a reference for any other purpose. The circuit diagram is subject to change without notice. </small> </p> <p data-bbox="653 963 739 971"> <small> Figure 13.14.8.14 Charge Pump 13 </small> </p>	Part:	05138-064G 3D NAND	Rev:	1.0	Author:	TECHINSIGHTS	Rev:	1.0	File:	05138-064G 3D NAND
Part:	05138-064G 3D NAND										
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Author:	TECHINSIGHTS										
Rev:	1.0										
File:	05138-064G 3D NAND										
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>										

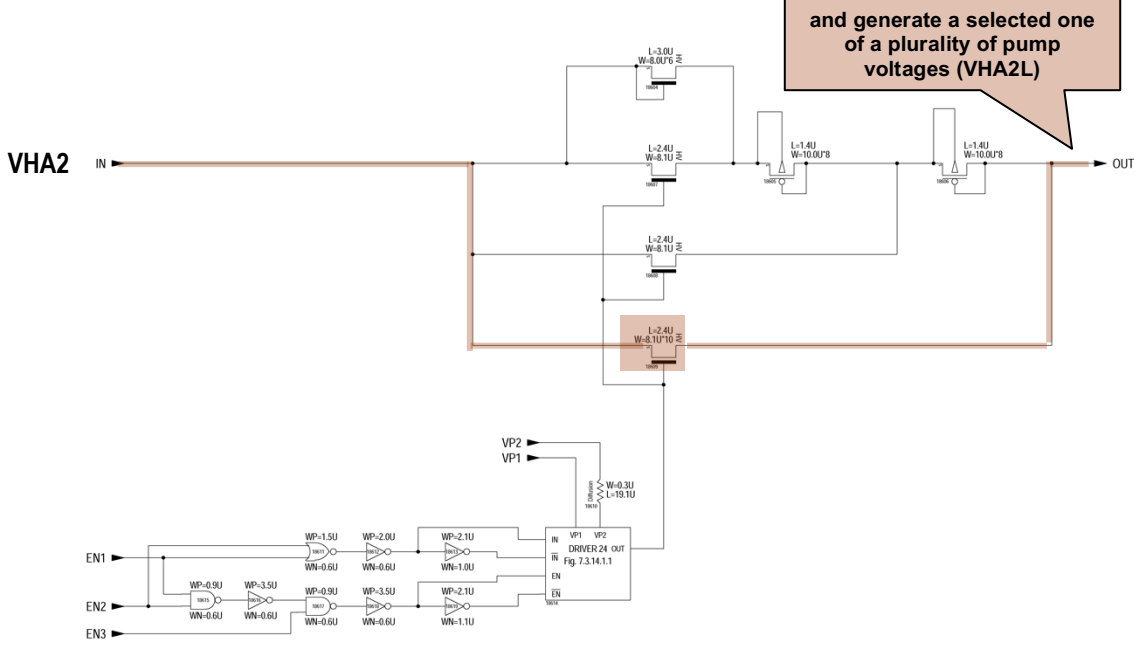
Claim 1	Accused Products
	 <p>comprising one or more stages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

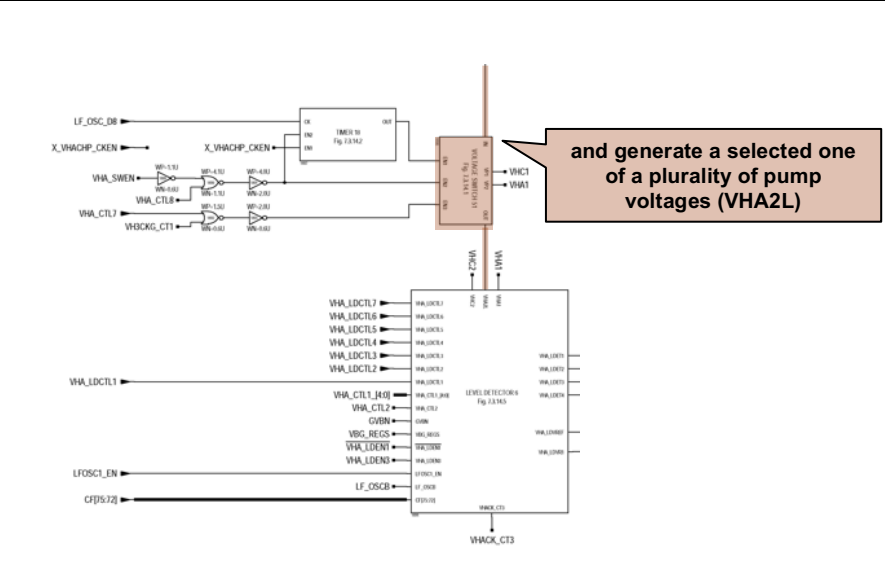
Claim 1

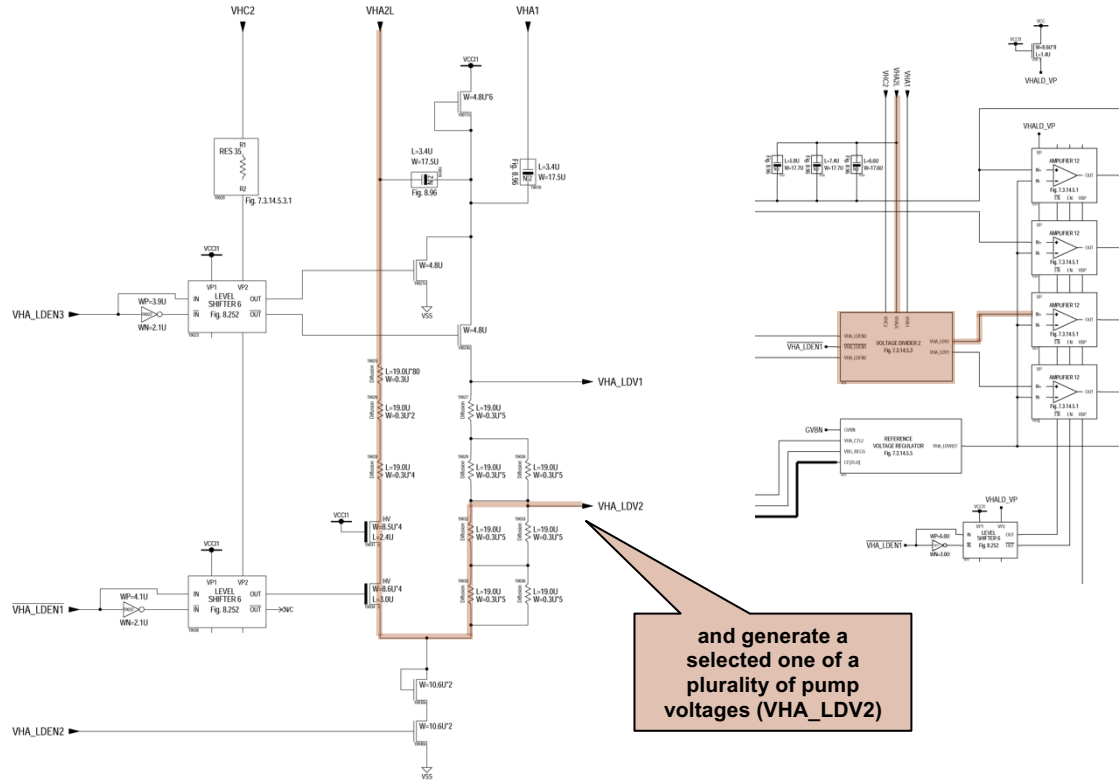
Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

Claim 1	Accused Products
	 <p>VHA2 IN</p> <p>OUT</p> <p>EN1</p> <p>EN2</p> <p>EN3</p> <p>VP2</p> <p>VP1</p> <p>and generate a selected one of a plurality of pump voltages (VHA2L)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>

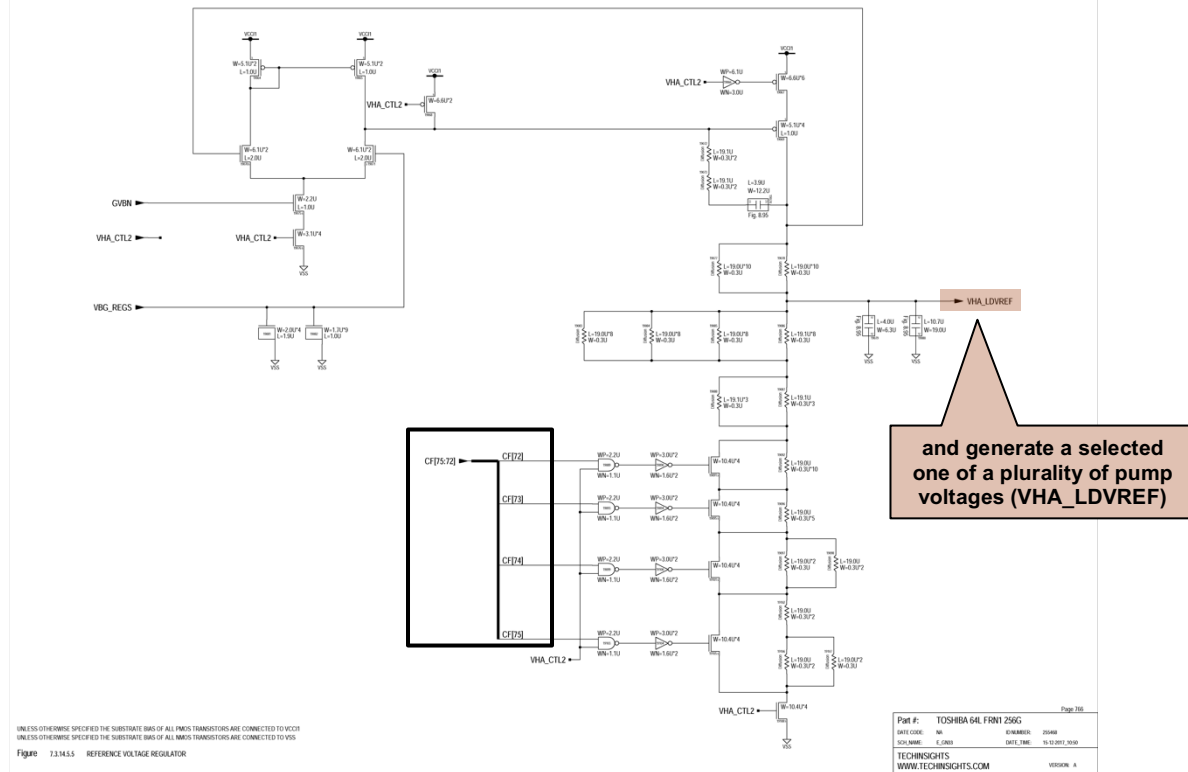
Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA2L)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA_LD2)</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

[illegible]

Claim 1

Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator

Claim 1	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

Claim 1

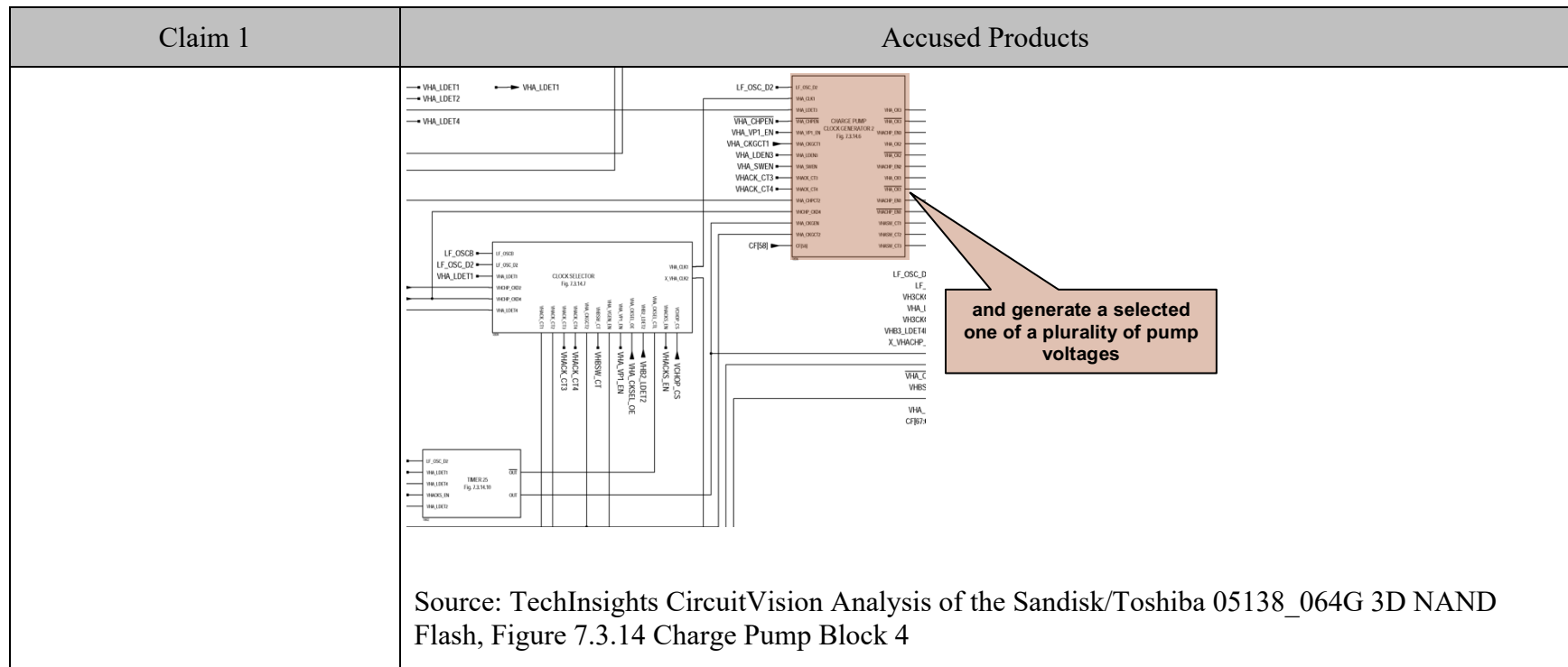
Accused Products

and generate a selected one of a plurality of pump voltages
VHA_LDET3 = 0

FIGURE 7.3.14.5 LEVEL DETECTOR 6

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6

Claim 1	Accused Products
	<p>VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p> <p>The circuit diagram illustrates the internal logic of the Charge Pump Clock Generator 2. It features several input signals at the top left, including VHA_OPEN, VHA_CKCT1, VHA_CKCT2, CFSR, VHA_LDEN, VHA_CHEN, VHAOK_CT4, VHAOK_CT3, VHA_LDET3 (highlighted with a red box), LF_OSC_DIV, VHA_CKGEN, VHA_CKOSC2, VHA_CLKM, and VHA_VPT_DIV. These inputs are processed by a series of logic gates (AND, OR, NOT) and multiplexers (labeled MUX0_01, MUX0_02). The output of the VHA_LDET3 signal path is highlighted in red, leading to a multiplexer that selects between different clock sources. This selected signal then branches out to multiple output pins labeled VHA_OK1 through VHA_OK6 on the right side of the diagram. A callout box points to one of these outputs with the text "and generate a selected one of a plurality of pump voltages".</p> <p>VHA_CK2 = 1 VHA_CK2* = 0</p> <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.6 Charge Pump Clock Generator 2</p>



Claim 1

Accused Products

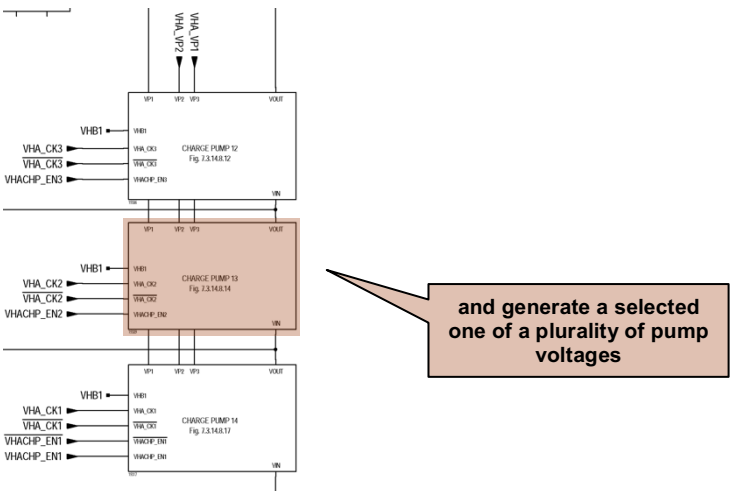
and generate a selected one of a plurality of pump voltages

a pumping circuit

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WWW.TECHINSIGHTS.COM

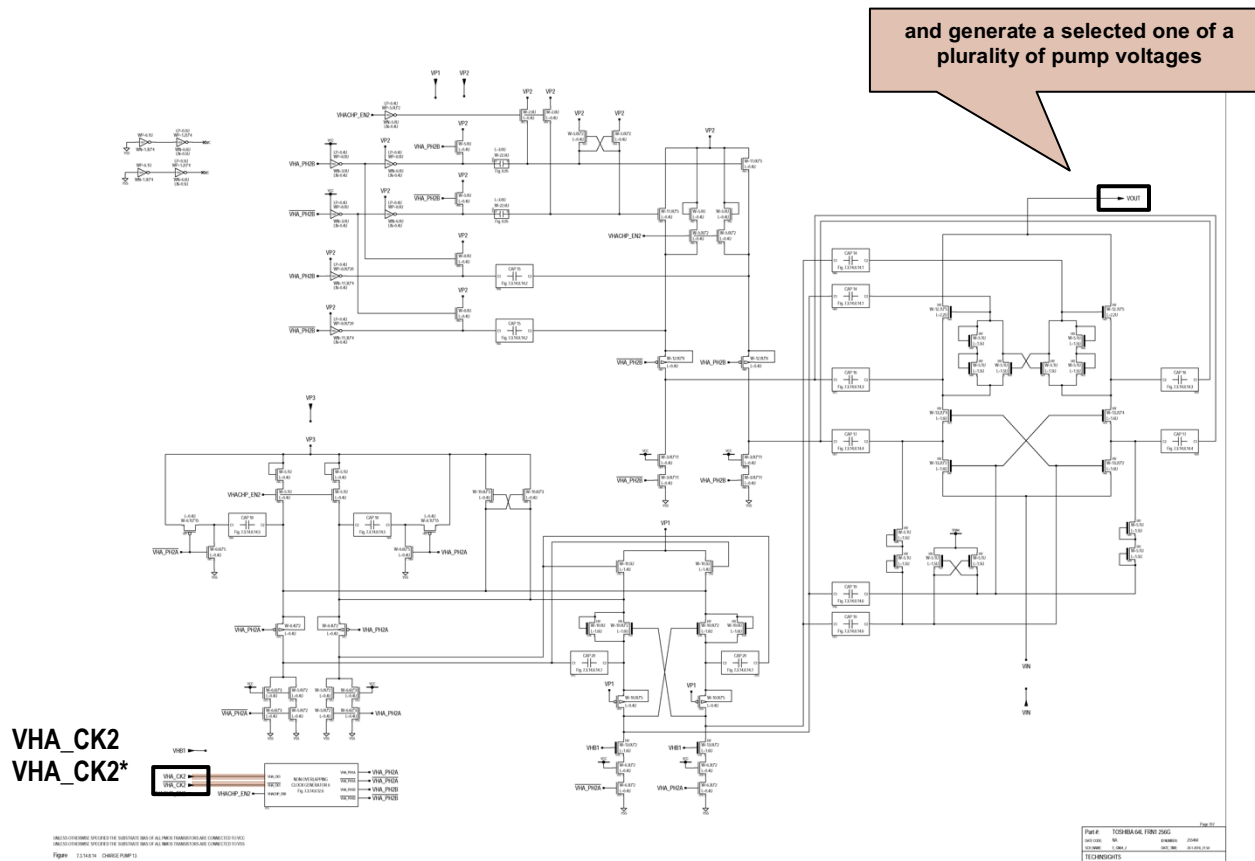
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Products

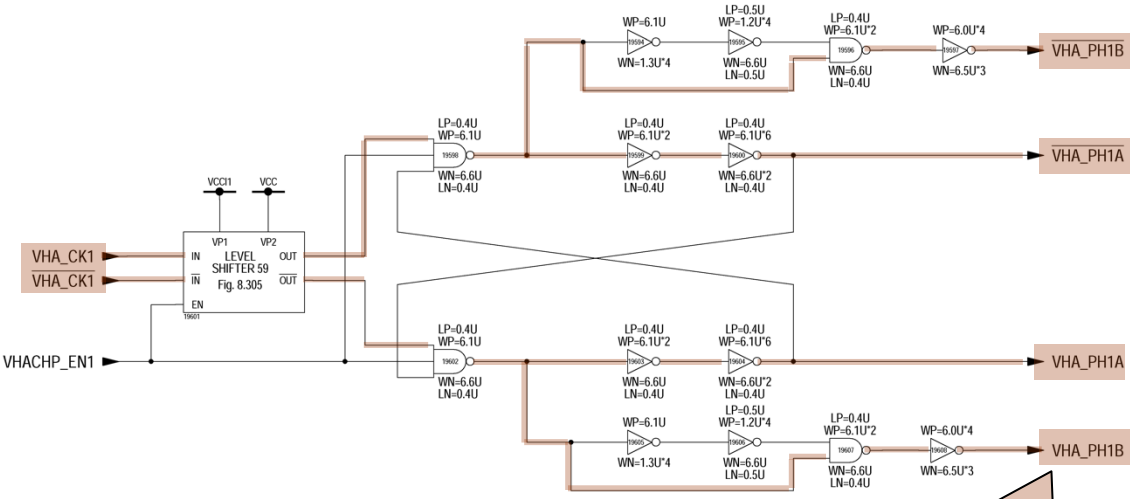
Claim 1	Accused Products
	 <p>The diagram shows three charge pump blocks stacked vertically. Each block has multiple input and output pins. The top block is labeled 'CHARGE PUMP 12 Fig. 7.3.14.8.12'. The middle block is labeled 'CHARGE PUMP 13 Fig. 7.3.14.8.14' and is highlighted with a red background. The bottom block is labeled 'CHARGE PUMP 14 Fig. 7.3.14.8.17'. A callout box with a pointer to the middle block contains the text: 'and generate a selected one of a plurality of pump voltages'.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

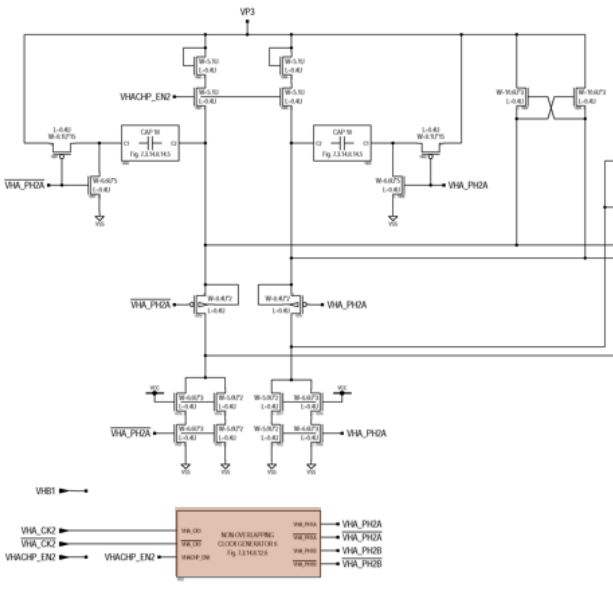
Claim 1

Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.13 Charge Pump 13

Claim 1	Accused Products
	<div data-bbox="636 355 758 417"> <p>VHA_CK2 VHA_CK2*</p> </div> <div data-bbox="1629 293 1766 417"> <p>VHA_PH2A VHA_PH2A* VHA_PH2B VHA_PH2B*</p> </div>  <div data-bbox="1533 951 1887 1018"> <p>and generate a selected one of a plurality of pump voltages</p> </div> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.12.6 Non-Overlapping Clock Generator 6</p>

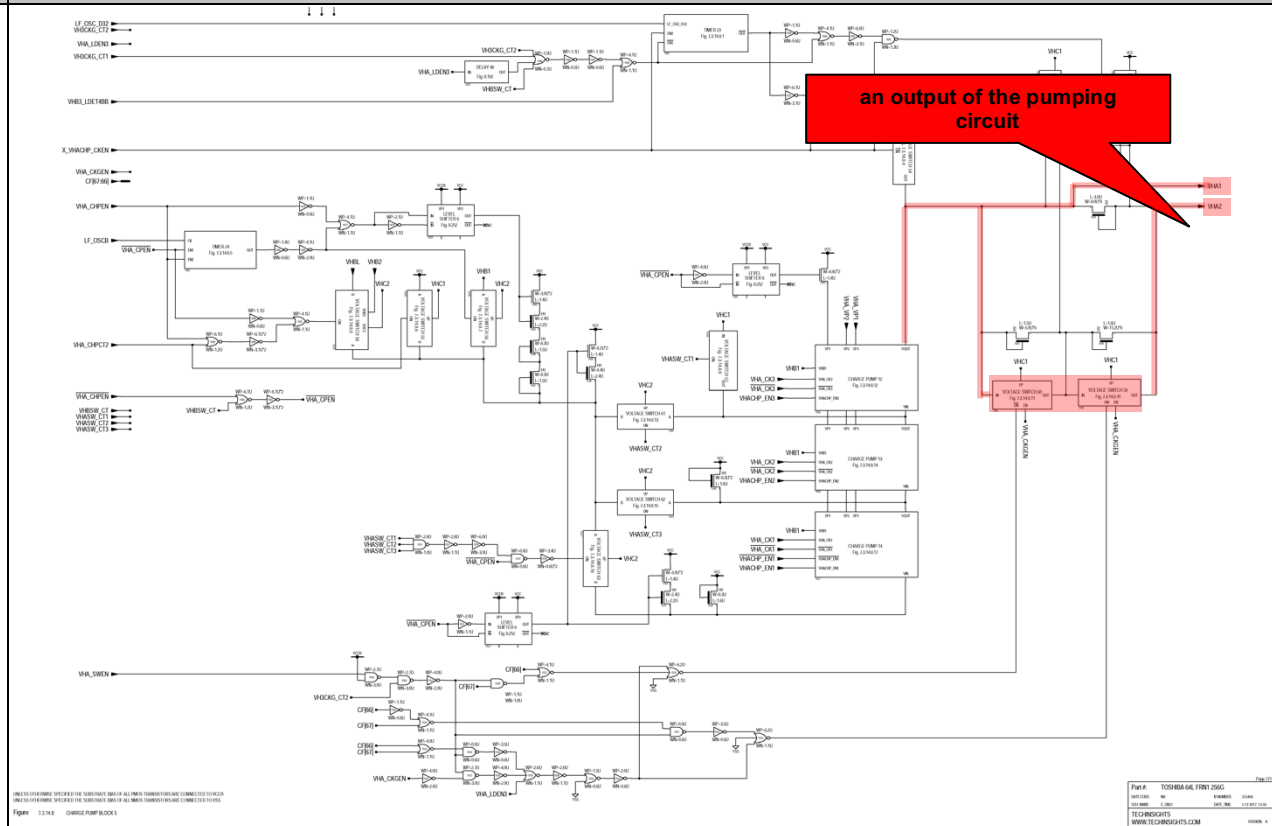
Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

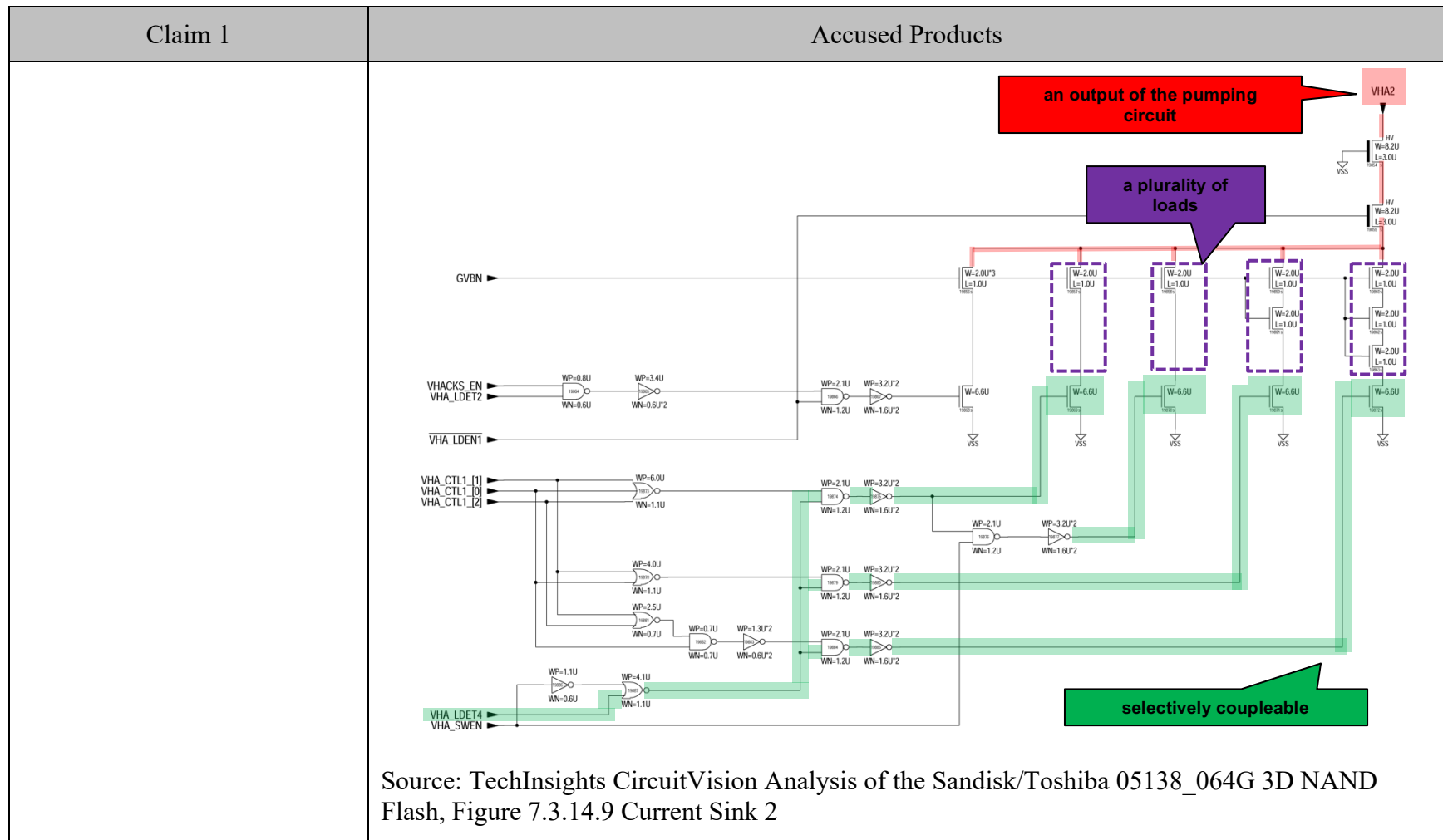
<p>Claim 1</p>	<p>Accused Products</p>
	<div data-bbox="1512 277 1873 440" style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p>and generate a selected one of a plurality of pump voltages</p> </div>

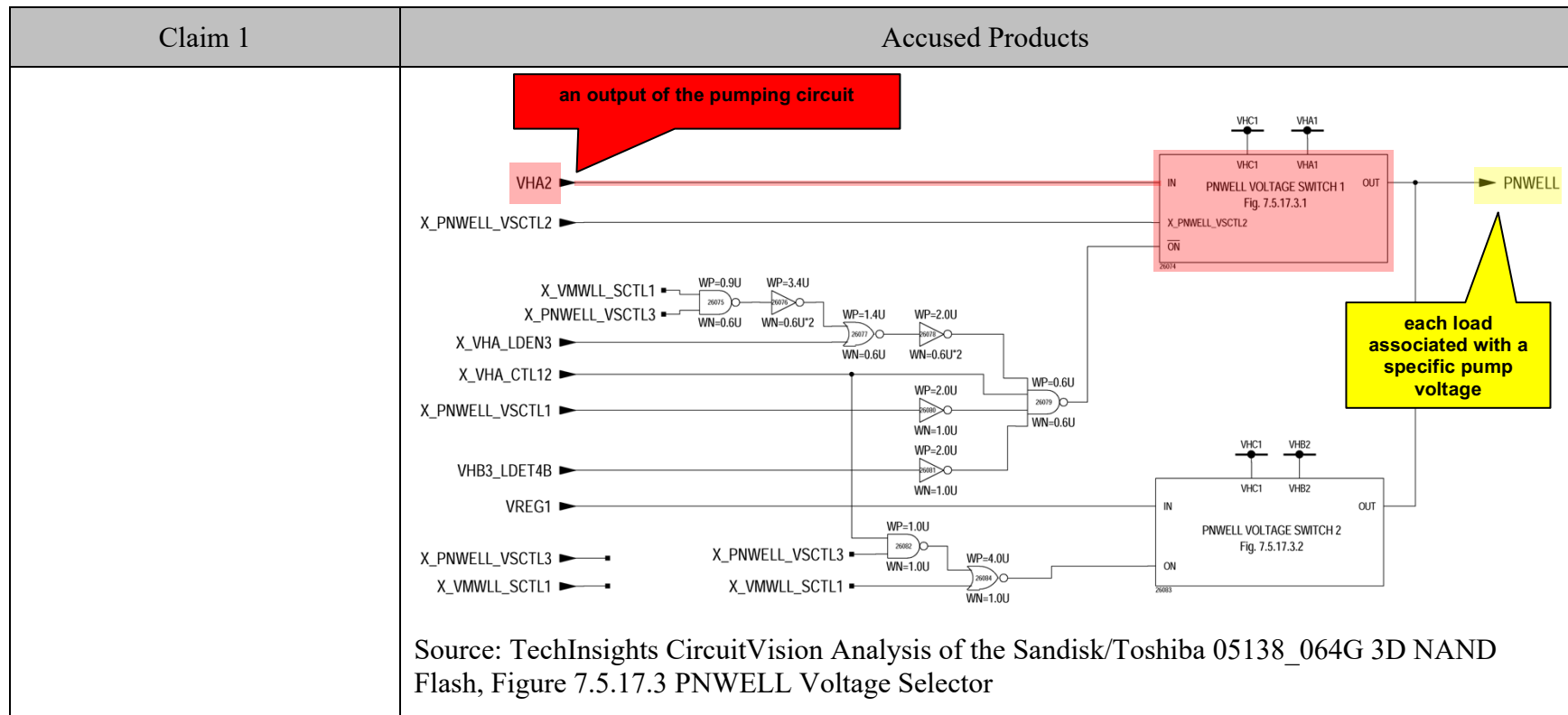
<p>Claim 1</p>	<p>Accused Products</p>
<p>[1b] b) a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and</p>	<p>Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.</p> <p>For example, VHA2 is an output of the pumping circuit of the WD Ultrastar SN630 WUS3BA196C7P3E3. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p>See, e.g.:</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

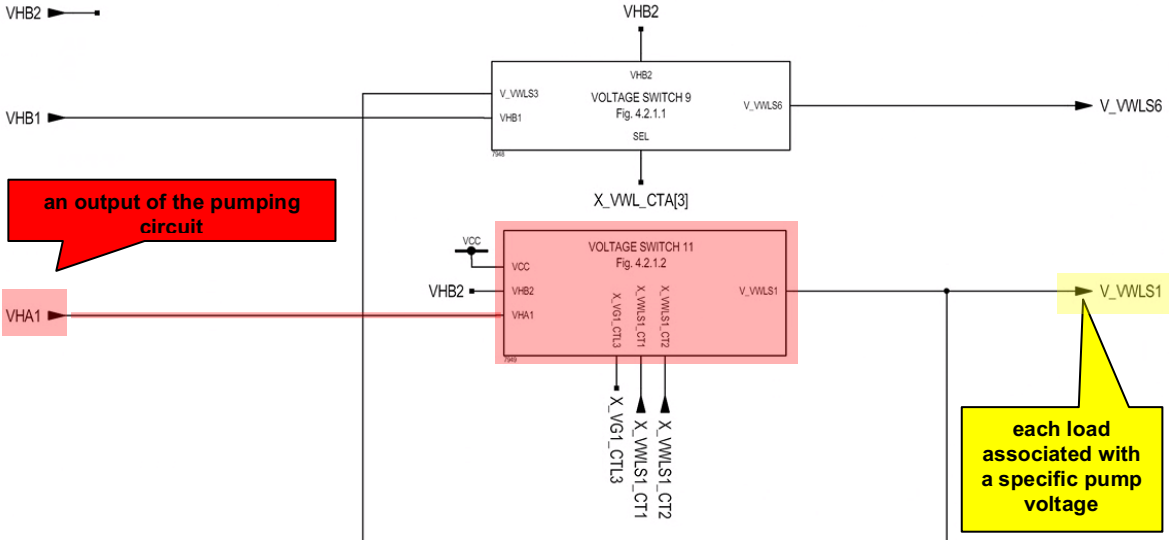
Claim 1

Accused Products



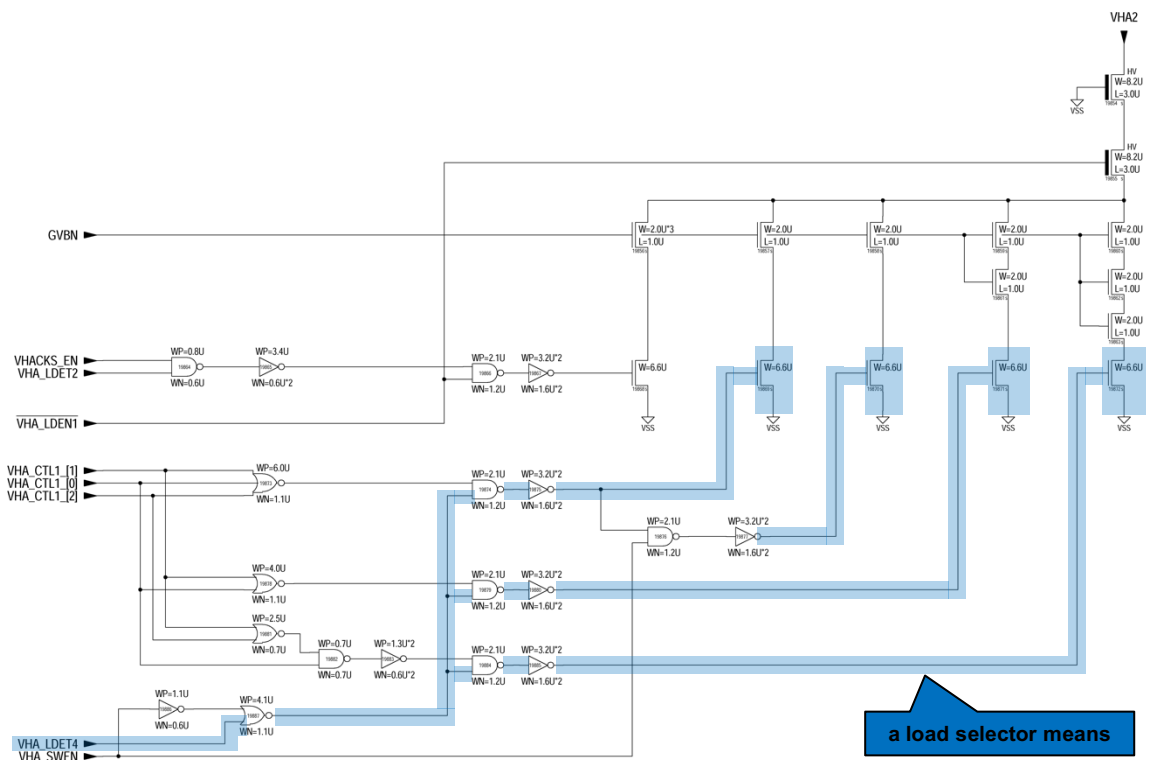


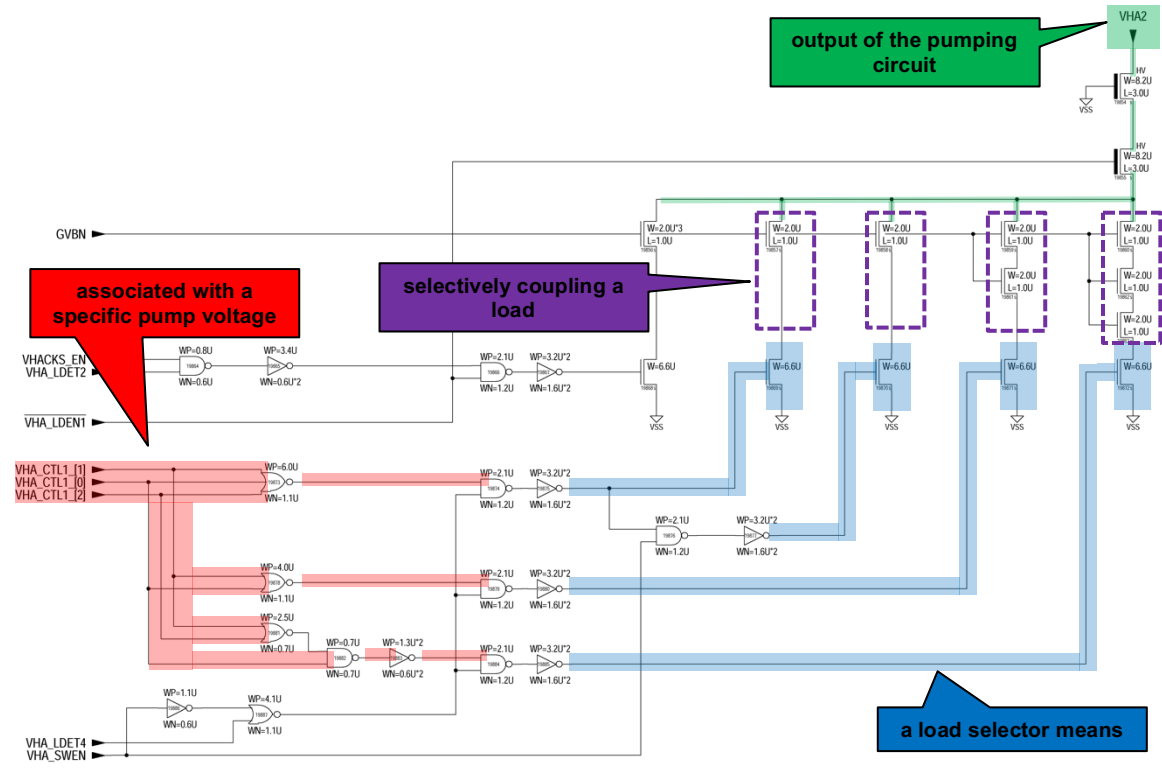


Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>[1c] c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, in the WD Ultrastar SN630 WUS3BA196C7P3E3, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3-bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

Claim 1

Accused Products

Claim 1	Accused Products
	 <p data-bbox="1512 993 1787 1039">a load selector means</p> <p data-bbox="632 1083 1829 1157">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Products
	 <p>The diagram illustrates a current sink circuit with several key components and annotations:</p> <ul style="list-style-type: none"> Associated with a specific pump voltage: A red callout points to the input signals <code>VHACKS_EN</code>, <code>VHA_LDET2</code>, and <code>VHA_LDET1</code>, which are connected to a network of PMOS (WP) and NMOS (WN) transistors. Selectively coupling a load: A purple callout points to a central control logic block that manages the coupling of different loads. Output of the pumping circuit: A green callout points to the output node <code>VHA2</code>, which is connected to a PMOS transistor (W=8.2U, L=3.0U) and a network of NMOS transistors. Load selector means: A blue callout points to the bottom right section of the circuit, which includes a PMOS transistor (W=4.1U, L=1.1U) and an NMOS transistor (W=1.1U, L=0.6U) that selects between different load paths. <p>The circuit also includes various other transistors with specified dimensions (W, L) and connections to <code>VSS</code> and <code>GVBN</code>.</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p> <p>For example, in the WD Ultrastar SN630 WUS3BA196C7P3E3, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], supra.</i></p>

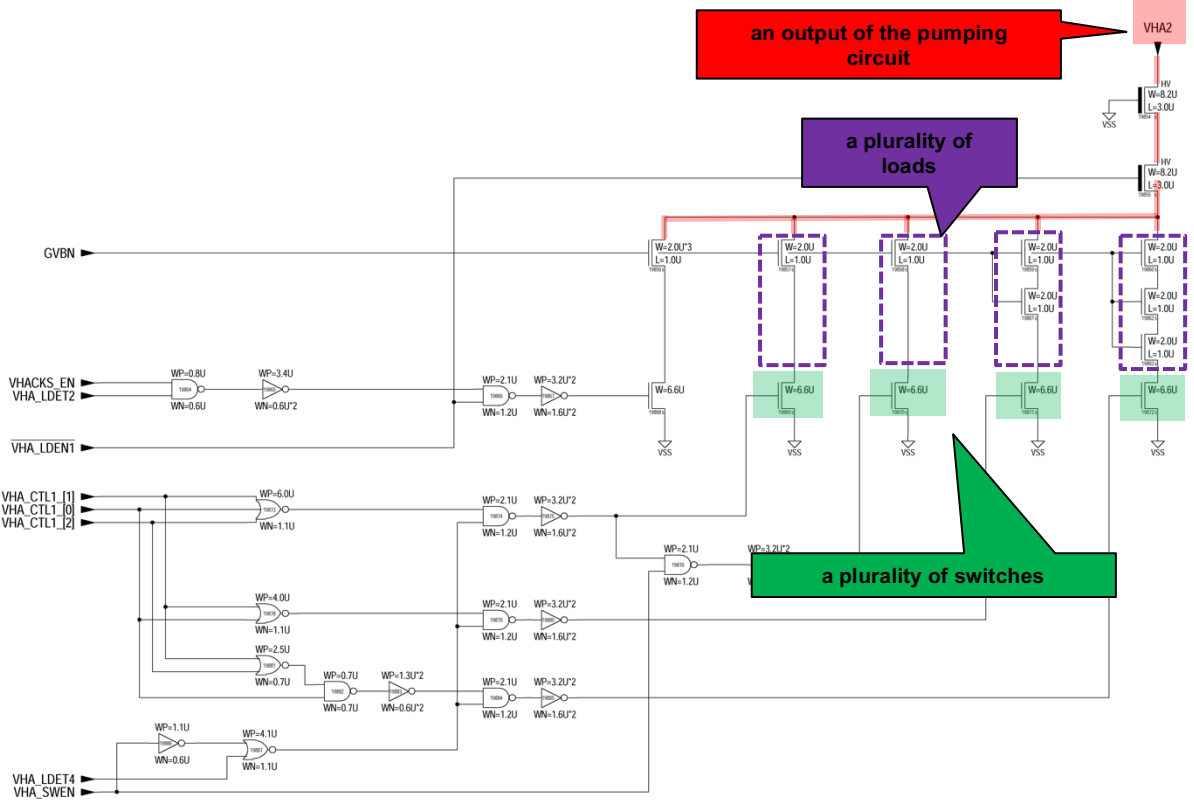
Claim 3

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, supra.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (V_{ref}).	

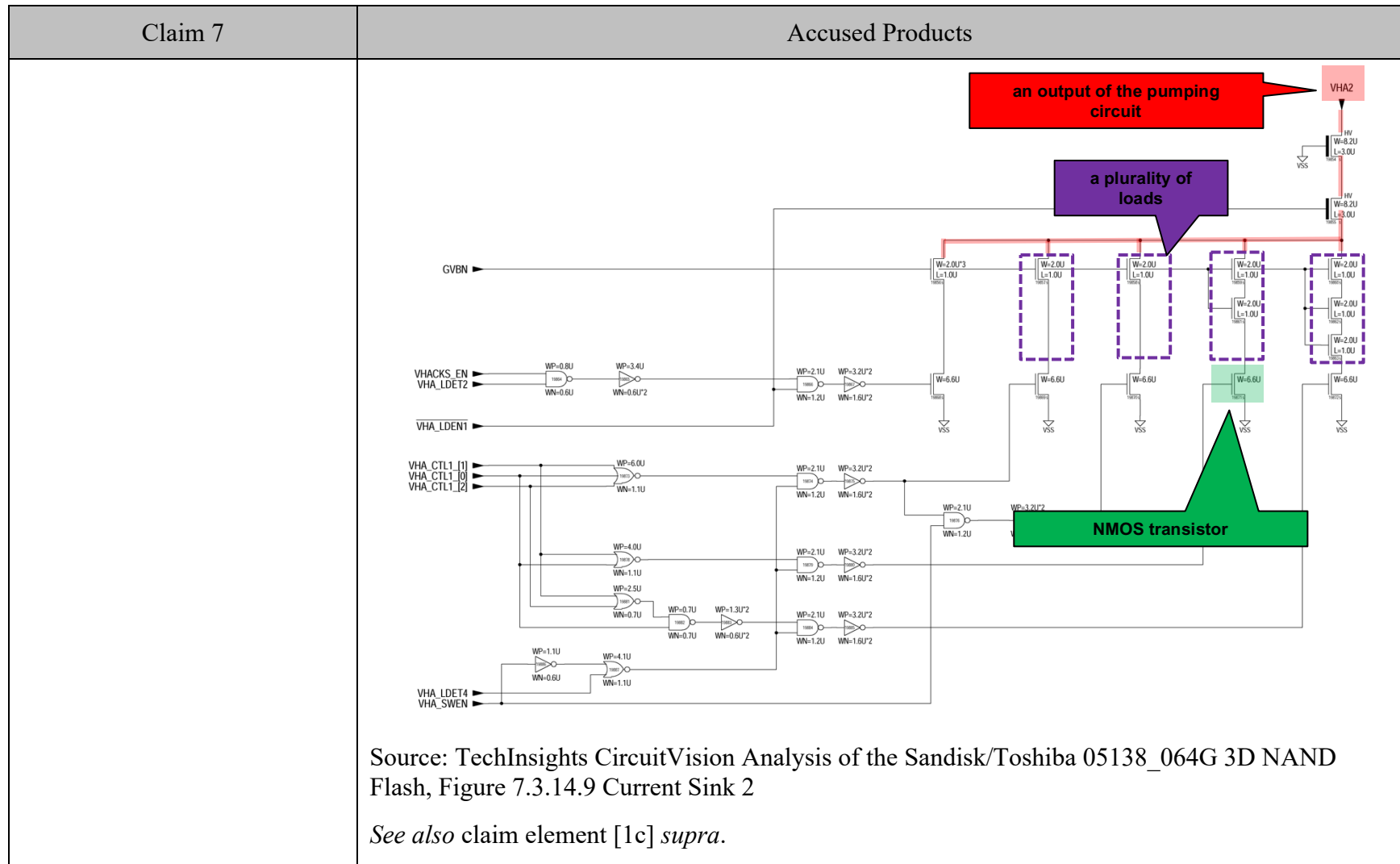
Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>

Claim 6	Accused Products
	 <p>an output of the pumping circuit</p> <p>a plurality of loads</p> <p>a plurality of switches</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p>See also claim element [1c] <i>supra</i>.</p>

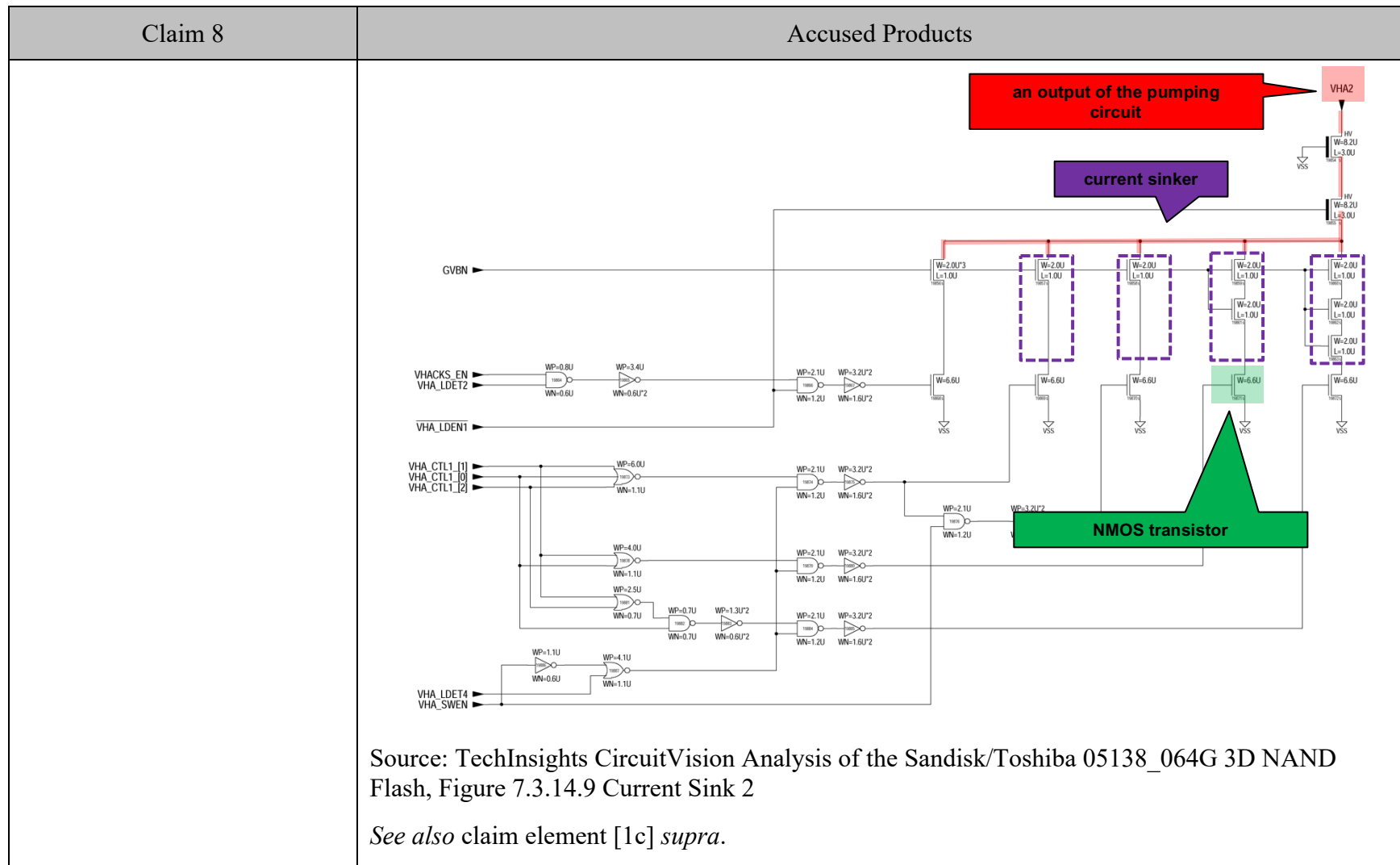
Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>



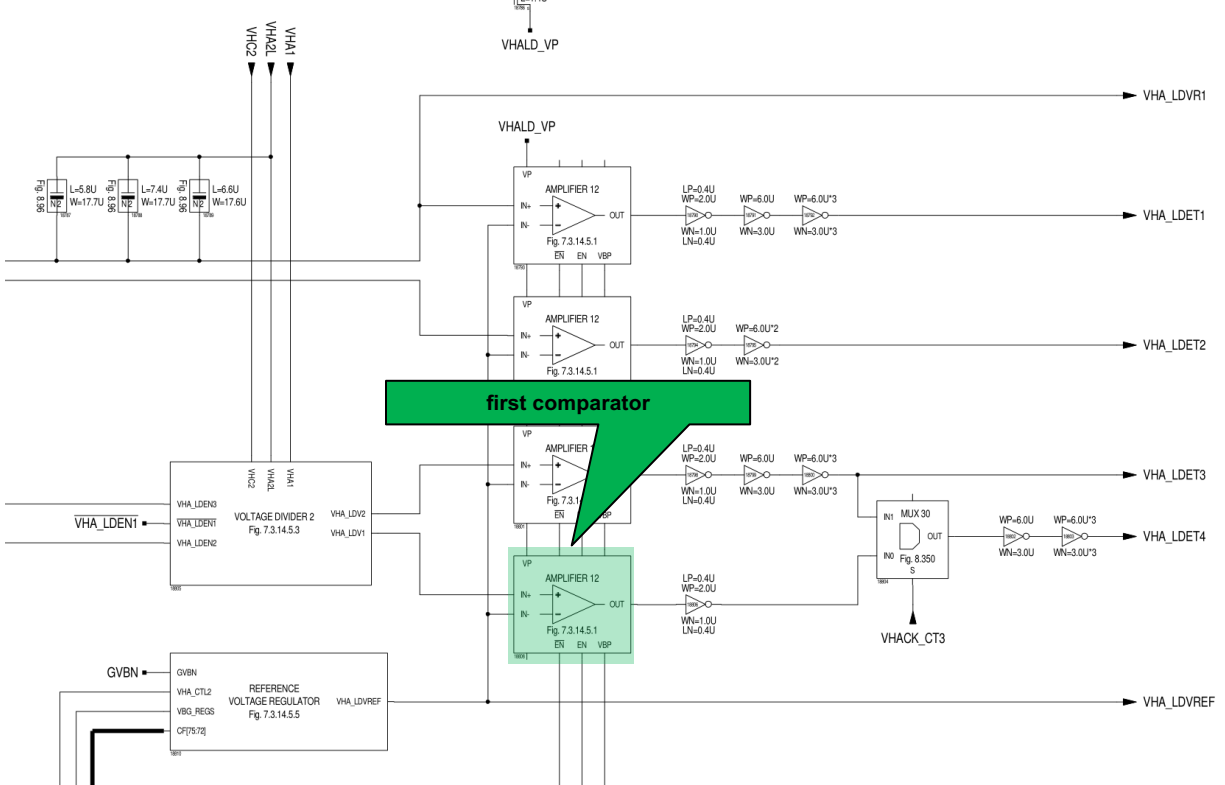
Claim 8

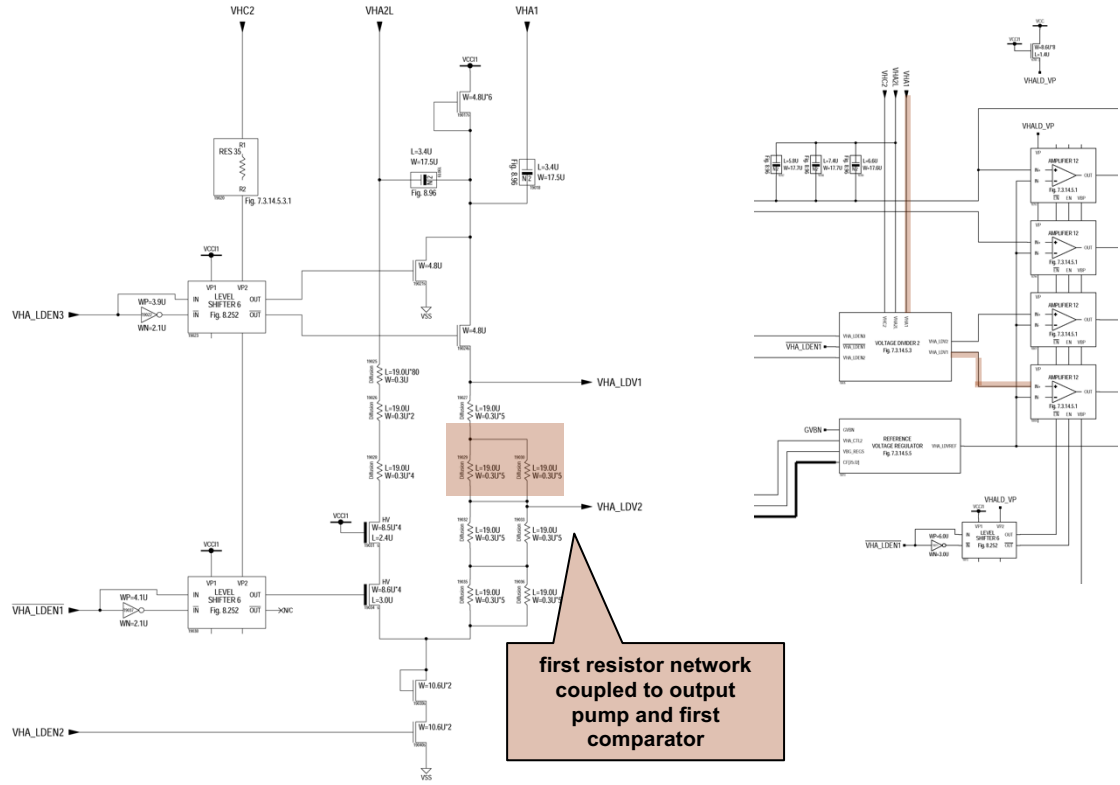
Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

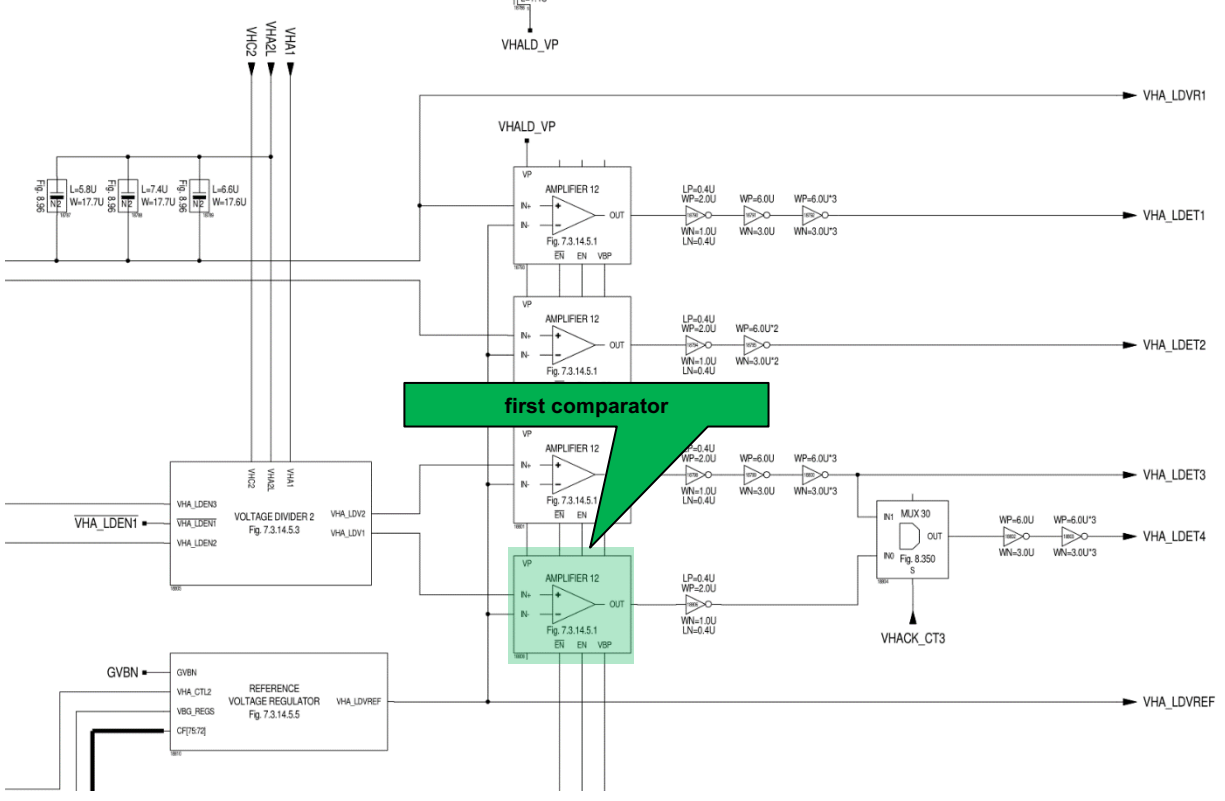


Claim 11

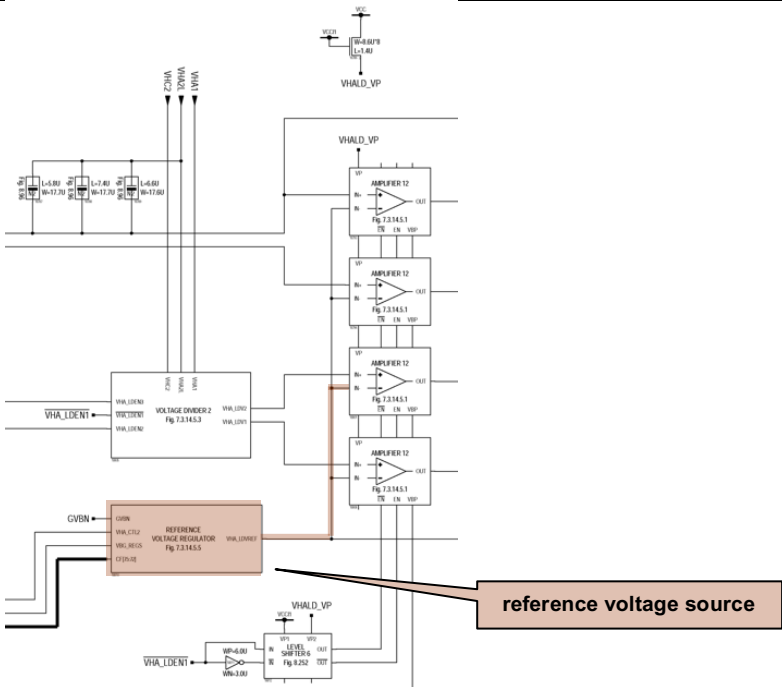
Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	Each Accused Product includes the charge pump circuit of claim 2. <i>See supra</i> claim 2.
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref). <i>See, e.g.:</i>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	 <p>first resistor network coupled to output pump and first comparator</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the</p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
<p>second resistor network being coupled to an electrical ground; and</p>	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
<p>[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p>	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p>See, e.g.:</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>